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# A New Method In Grid Interconnecting Solar Generation System Using Multilevel Inverter

## [1]C.PRAVEEN,[2] P.KISHORE RAJU

[1]Assistant Professor, EEE Dept., CR Engineering College, Tirupathi, Chittoor (Dist) A.P, India,
[2]II M.Tech (PE&D) Student, CR Enineering College, Tirupathi, Chittoor(Dist) A.P, India,
[1]praveenchukkala37@gmail.com ,[2]kishorepydikondala@gmail.com

**Abstract:**
Now a days generation of electrical energy is concentrating more on renewable energy sources i.e., wind&solar. While interconnecting the renewable energy generating station with grid we are facing problems with powerquality due to fluctuations in generation by wind and solar.
In this paper I am going to interconnect the solar generation system with grid using multilevel inverter concept. To interconnect with grid or utility system I am using one converter, one 7-level inverter and transformer. The converter is a dc/dc power converter consisting of boost converter and a transformer to convert the output voltage of the solar cell array into two independent voltage sources having multiple relationships. The capacitor selection in this multilevel circuit produces the dc output voltage as a 3-level dc voltage and then the full bridge powerconverter converts this 3-level dc voltage into 7-level ac voltage.
The generated voltage in the above scheme will be a sinusoidal one and will be in phase with the grid voltage and is given into the utility.
The main and excellent thing proposing in this paper is that I am using only 6-power electronic switches to generate a 7-level multi-level inverters
**INDEX TERMS***: Power Converter, 7-Level Multilevel Inverter, PLL, PWM Generator,MATLAB.*

## I. INTRODUCTION

The greenhouse emissions problems are resulting in the globe due to the usage of fossil fuels. By considering this as the cause the total globe is going to use the solar power generation system instead of using the fuel cells Which produces less pollution as well as the cost required is less. Particularly in domestic uses the solar power generators are going to play a major role in near future.

In interconnecting the solar power generation system with the grid the conversion of grid is more considered one. In solar power generation system the generated power is D.C and the grid or utility requires the A.C so while converting the DC to AC requires power conversion technique to feed the A.C utility. As the voltage generated by the solar cell is low in magnitude so we require a dc-dc voltage converter to step-up. The dc output voltage so that it can match the input voltage of the inverter.

The efficiency of the power converter is important to ensure that there is no waste of energy generated by using the solar power generator. Both the active and passive devices in the inverter will cause the more losses which includes both the switching and conducting losses i.e., conduction

losses will result from the use of active device. Where switching losses will result from in proportional to the voltage and the current changes for each switching frequency. To overcome the switching harmonics we are using the inductive filter. So that power loss is proportional to the amount of switching harmonics.

In order to improve the power converter efficiency the voltage at each switching operation of the multi-level inverter is reduced. So that the switching stress on the active device gets decreased. By doing this the amount of switching harmonics will get reduced. So the power loss caused by filter inductor will also reduced.

In this case from past many years most researches have been goingon on the multilevel inverter topology. In present project to reduce harmonic content and electromagnetic interference(EMI) and to increase the efficency the high voltage levels are generated.

In general multilevel inverters mainly consisting of diode-clamped, flyback capacitor and the cascade H-Bridge. In the above diode-clamped and flyback capacitor multilevel inverters usage of capacitors develop several voltage levels. But it is difficult to regulate the voltage of these capacitors since it is

difficult to create an asymmetric voltage technology and also the circuit designed is also complicated as we increase the voltage levels. For single phase and 7-level inverter 12-power electronics switches are needed in both the types of the devices where as in the H-Bridge inverters produces 7-level voltage by using the multiple relationships and eight power electronic devices are needed. Most recently various types of new methods have been arrived in reducing the complexity in switching devices for 7-level multilevel inverters. For Example, a single –phase seven level grid connected inverter has been developed for photovoltaic system[09]. In this grid connected inverter contains six power electronic switches but in this three capacitors are used to construct the three voltage levels, which results in that balancing the voltage levels, which results in that balancing the voltages of the capacitors is more complex. In [10], a seven-level inverter topology, configured by a level generation part and a polarity generation part is proposed. In this project power electronic switches in level generation part is in high frequency as well as the usage of power electronic switches are ten which is making more and more complexity. In [11] a modular multilevel inverter with a new modulation method is applied to the photovoltaic grid-connected generator. This modeled inverter is similar to H-bridge type of inverter. For this to achieve dynamic voltage balance a new modulation method is proposed. In [12], a multilevel dc-link inverter is presented to overcome the problem of partial shading of individual photovoltaic sources that are connected in series.the dc bus of a full- bridge inverter is configured by seversl individual dc blocks, where each dc block is compared of a solar cell, a power electronic switch, and a diode. Controlling the power electronics of the dc block will result in multilevel dc-link voltage to supply a full- bridge inverter and to simultaneously overcome the problems of partial shading of individual photovoltaic sources. So to overcome all the problems resulting in the above projects I am going to propose a new method which is given below.

## II. PROPOSED SYSTEM

In this project I am proposing a new solar generation system. This system comprising of a dc/dc power converter, and a seven-level inverter. In this 7-level inverter the output is obtained using a capacitor selection circuit and a full bridge power converter connected in series. In this proposed system we are using only 6-power electronic devices as switches to generate the 7-level output voltage. And in the power electronic switches configured in such a manner that only one power electronic switch is switched at high frequency at any time to generate

the 7- level output voltage. The switching power loss is reduced and the power efficiency is improved The below figure shows the proposed solar power generation system with the multilevel inverter.
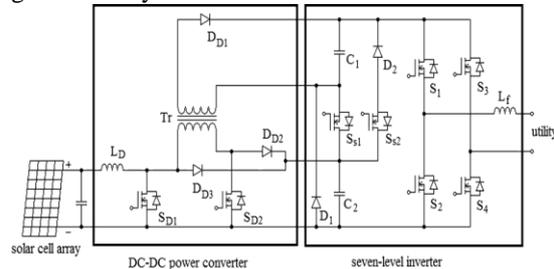


Fig (1): Proposed Grid interconnected Solar Power Generation System

In this proposed system a solar cell array, a dc-dc power converter, and a new 7-level inverter. The solar cell array is connected to dc-dc power converter consisting of a stepup converter connected with a transformer having a turns ratio of 2:1. This dc-dc power converter converts the output power of solar power array into two independent voltage sources with multiple relationships, giving to the 7-level inverter. The new 7-level inverter is configured with capacitor selection and a full-bridge power converter are connected in series. Due to the multiple relationship in capacitors voltage can discharge individually or in series consisting of 3-level D.C output voltage. The 3-level D.C voltage will be given to the multilevel inverter and this inverter will generate the output as the a.c 7-level inverter which can synchronize with the utility voltage. In the above Explained process will generate the A.C voltage from a solar power array to synchronize with grid. In this proposed circuit the power circuit used in this can get simplified with the usage of 6-power electronic switches.

## III. DC-DC POWER CONVERTER

The dc-dc power4 converter consisting of boost converter and a current- fed forward converter charging both the capacitors c1 and c2 . Capacitor c1 is charged by using the current-fed forward converter. The current fed forward converter consist of inductor LD,SD1,SD2, Diode DD1,DD2 and a Transformer. Capacitor c2 is charged by using the boost converter comprising of inductor LD, Power electronic switch SD, and Diode DD3.

## IV. OPERATION OF DC-DC POWER CONVERTER

When power electronic switch SD1 is turned ON the capacitor c2 will charge by using the DC-DC power converter which is shown in figure 2(a).
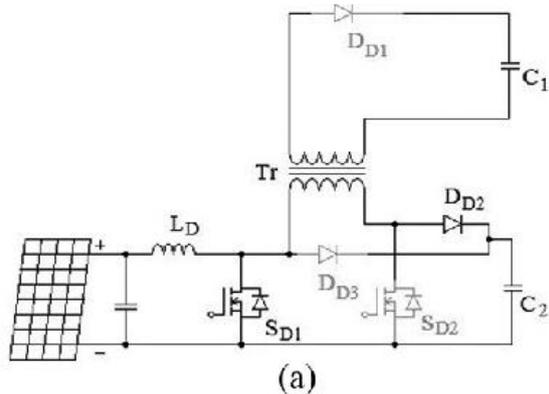
FIG 2(a):Operation power converter when switch SD2 is OFF

If the power electronic switch SD2 is turned on the capacitor c1 will get charged by using the solar power generation system energy to the inductor LD, switch SD1 is turned Off, which is shown in fig2(b).
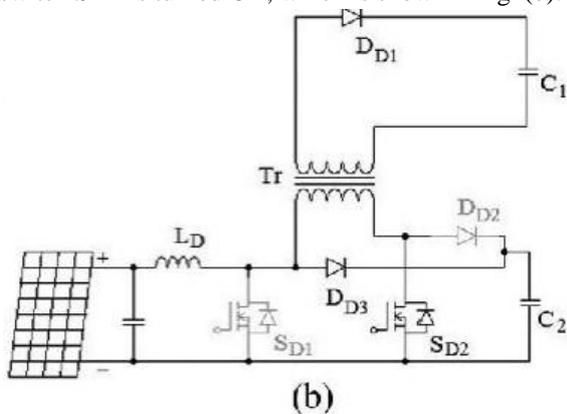


FIG 2(b):Operation power converter when switch SD1 is OFF

Capacitor c1 and capa itor c2 are connected in parallel through the transformer. In such a way tha the energy of inductor LD and the solar cell array charges capacitor c2 through diode DD3 and charges capacitor c1 through the transformer and diodeDD1 during the Off state.

By using the transformer we can charge the capacitor c1 and c2 in parallel, the voltage ratio of capacitor charging is same as the transformer ratio of 2:1.

The boost converter is operated in continuous conduction mode (CCM) charging the capacitor c2 which is given by $V_{c2}= (1/(1-D)) V_s$

$V_s$= output voltage of solar cell array D= duty ratio of SD1

The capacitor c2 voltage is given by $V_{c1}=(1/2(1-D)) V_s$

When the switch SD2 is in ON state then the magnetizing inductance of the transformer increases. in normal case to reduce these magnetizing inductances are sent back to the source by using the third demagnetizing winding. However in proposed system the magnetizing inductance is delivered to the capacitance c2 through the DD2 and SD1 when SD2 is turned OFF. Since the energy stored in the magnetizing inductance is transformed forward to the output capacitance c2 and not back to the dc source by doing this power efficiency also increases.

## SEVEN-LEVEL INVERTER

As already said the seven level inverter is a combination of capacitor selection circuit and a full-bridge power converter connected in series. The operation involves in output production as +ve and output as –ve. For analyzing the circuit the circuit switches are treated as ideal while the voltages of both capacitors c1 and c2 in the capacitor selection circuit are constant and equal to Vdc/3 and 2Vdc/3 respectively.

The operation of during +ve half cycle is divi 7-level inverter ed into 4-modes as shown in the below analysis

### +Ve Half Cycle Analysis:

### Mode 1:

In this mode of operation the output of the seven level inverter should be Vdc/3. We can obtain the output by bringing the switches SS1 and SS2 to OFF state in capacitor selection circuit and the switches S1 and S4 in power converter circuit are bringing to the conduction state i.e., ON state. Here the capacitor circuit output voltage is directly feeded to the power converter and the full-bridge will produce output which is equal to the Vdc/3
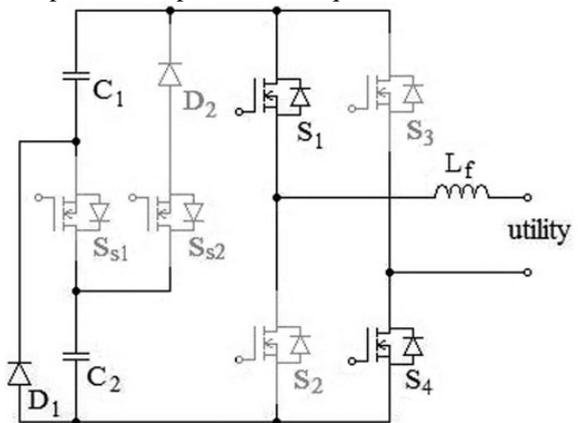


### MODE2:

The output of the power converter circuit in this mode of operation is 2Vdc/3. During this mode of

operation the 7-level inverter will be operated in such a way that SS1 is Off and SS2 is ON, so c2 is discharged through SS2 and D2, the output voltage of the capacitor selection circuit is 2Vdc/3. During this mode S1 and S4 of the full- bridge power converter are ON producing the ouput of the inverter to the 2Vdc/3.
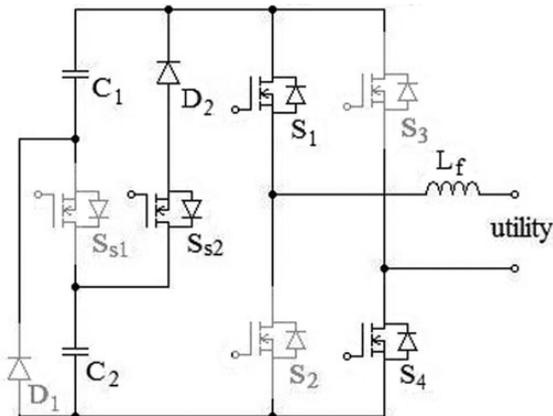


## MODE3:

The output of the multi level inverter in this mode of operation is Vdc. In this type of operation SS1 is ON and D1 is reverse biased. The switch SS2 in capacitor selection circuit will not affect the current flow in the capacitor selection switch. Both c1 and c2 are discharged in series and the output voltage of the capacitor selection circuit is Vdc. Resulting in production of output voltage as Vdc the power converter switches S1 and S4 are bring to the conduction state.
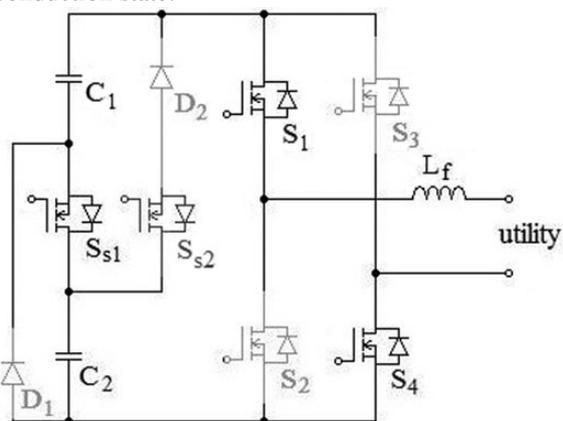


## MODE4:

In this mode of operation both SS1 and SS2 are Off in the capacitor selection circuit resulting in the output voltage of Vdc/3. In this mode only S4 of the full bridge power converter is ON. As the output of the 7-level inverter is +ve and passes through the filter inductor forcing the anti-parallel diode of S2 to be switched ON for continuous conduction of the filter
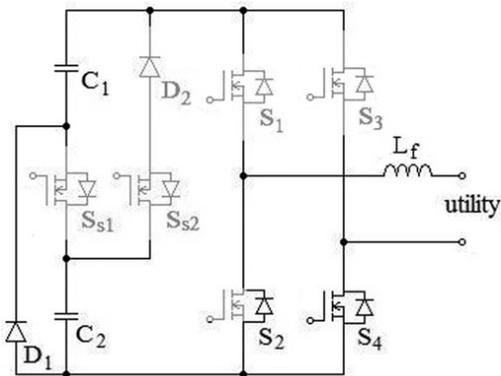


inductor current. Which results in output voltage of the proposed 7-level inverter is zero.

From the above mode of operation we can say the out put voltage of the 7- level inverter have 4 level in magnitude of voltage they are Vdc, 2Vdc/3, Vdc/3 and 0.
The output of the 7-level inverter should be synchronized with the grid or utility voltage when the –Ve half cycle is present. So to make synchronization we are going for the –Ve half cycle operation.
Similar to the +Ve halfcycle operation –Ve half cycle also will have the same 4 modes. In this modes of operation the capacitor selection circuit in the –Ve half cycle is same as that in the +ve half cycle. The only difference is that in +ve half cycle S1 and S4 are acting in the full bridge converter But in –Ve mode it is the function of S2 and S3. During the first 3 modes of operation s2, s3 are in ON state (i.e., 5,6,7 0, ans S2 is onlt the device that will be in conduction during mode 8 of the –Ve half cycle. So the output voltage of the 7-level inverter also have the 4-levels of magnitude in output i.e., -Vdc,-2Vdc/3,-Vdc/3 and 0. Which will be shown in the below figure.

From the operation of 7-level inverters we can find that there are 7-levels of magnitude whose output is Vdc, 2Vdc/3, Vdc/3, 0, -Vdc/3, -2Vdc/3,-Vdc/3 and –Vdc
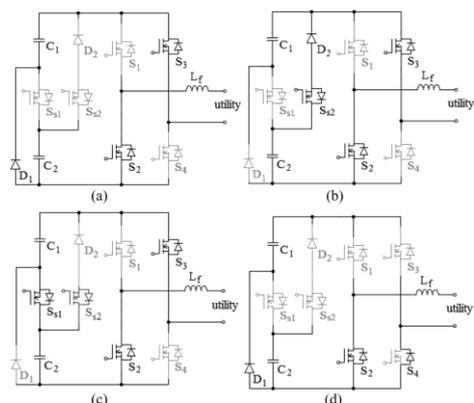
## V. CONTROLLING OF 7-LEVEL INVERTER

In this controlling will be done by the current mode of control and PWM is used to generate the controlling signals for the power electronic switches In order to satisfy the synchronizing of grid with Solar Poer generation system we have to control the output of the inverter with in 2-levels that is in one level the output of the inverter must be higher than the utility voltage to increase the filter inductor and in another level the voltage must be more less than the utility voltage in order to reduce the filter inductor current.

The output voltage of the inverter must be changed with respect to the utility voltage by considering the refverance current from the controlling

During +Ve half cycle conduction the utility voltage is smaller than Vdc/3. The multilevel inverter must be switched between modes 1 and 4 to a output voltage of Vdc/3 or 0. Within this voltage range S1 is switched in PWM, so the duty ratio d of s1 can be represented as

$d = V_m/V_{tri}$

$V_m$ = modulation signal

$V_{tri}$ = amplitude of carrier signal in pwm circuit

the output voltage of 7-level inverter is given by

$Vo = d * Vdc/3 = K_{pwm} * V_m$

$K_{pwm}$ = gain of inverter

$K_{pwm} = Vdc/(3 * V_{tri})$

The below figure shows the simplified model for the 7-level inverter when the utility voltage is smaller that Vdc/3. The closed loop transfer function is given by

$$I_o = \frac{k_{pwm}\, G_c/L_f}{s + k_i k_{pwm} G_c /L_f} I_o - \frac{1/L_f}{s + k_i k_{pwm} G_c /L_f} V_u$$

Where $G_c$ is the current controller and $K_i$ is the gain of the current detector
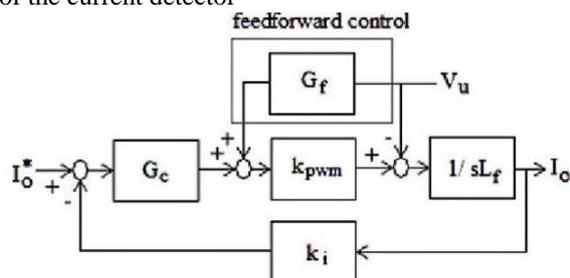


If the utility voltage is in the range (Vdc/3, 2Vdc/3) then the 7-level inverter is switched between modes 2 and 1. To gain the voltage range SS2 is switched in pwm so the duty ratio SS2 is same as the above switch so the output voltage is

$vo = d \cdot Vdc/3 + Vdc/3 = k_{PWM}Vm + Vdc/3.$

And the closed loop transfer function for the above range of utility voltage is shown in figure
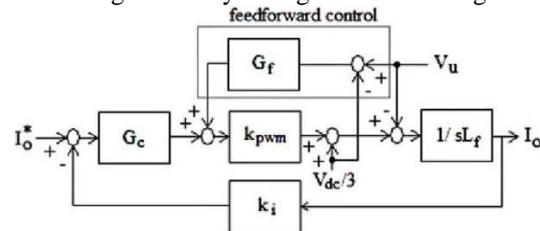


The closed loop transfer function is derived as

$$I_o = \frac{k_{pwm}\, G_c/L_f}{s + k_i k_{pwm} G_c/L_f} I_o^* - \frac{1/L_f}{s + k_i k_{pwm} G_c/L_f}(V_u - V_{dc}/3).$$

When the utility range of (2Vdc/3, Vdc) then the 7-level inverter must be switched between modes 3 and 2. To obtain this voltage range the switch SS1 is switched in PWM and SS2 remains in the ON state to avoid switching of SS2. Then the output voltage is given by.

$Vo = d \cdot Vdc/3 + 2Vdc/3 = Kpwm*Vm + 2Vdc/3.$

The closed loop controlling for this mode of operation is shown below

And the closed loop transfer function is shown
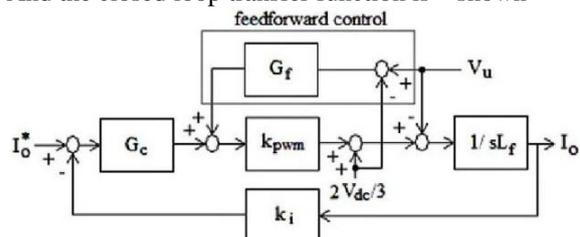


Below

$$I_o = \frac{k_{pwm}\, G_c/L_f}{s + k_i k_{pwm} G_c/L_f} I_o^* - \frac{1/L_f}{s + k_i k_{pwm} G_c/L_f}(V_u - 2V_{dc}/3).$$

From the above all transfer function we can say that the second term is disturbance. In order to eliminate that disturbance the feed forward controlling is used having the gain Gf is KPWM

Till now we have controlled during +Ve half cycle. In the –Ve half cycle also the same feed forward controlling is used to obtain the utility range voltages. In order to have the output voltage of –Vdc/3 or 0. The switch s3 is switched in PWM and the 7-level inverter is switched in mode 6 and 5 to a output voltage of

-2Vdc/3 or –Vdc/3

By comparing the proposed system with the nominal or normal converters we can say that the level of

complexity is reduced as we are using only 6-power electronic switches for 7- level output voltage. All the range of utility voltages for operating the 7-level inverter is placed in table which is shown below

| positive half cycle | | | | | | |
|---|---|---|---|---|---|---|
| | $S_{S1}$ | $S_{S2}$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ |
| $|v_u| < V_{dc}/3$ | off | off | PWM | off | off | on |
| $2V_{dc}/3 > |v_u| > V_{dc}/3$ | off | PWM | on | off | off | on |
| $|v_u| > 2V_{dc}/3$ | PWM | on | on | off | off | on |
| negative half cycle | | | | | | |
| $|v_u| < V_{dc}/3$ | off | off | off | on | PWM | off |
| $2V_{dc}/3 > |v_u| > V_{dc}/3$ | off | PWM | off | on | on | off |
| $|v_u| > 2V_{dc}/3$ | PWM | on | off | on | on | off |

**Power electronic switches conduction states during the utility voltage Ranges**

In the above table we can observe that in all the cases only 3 power Electronic switches are conducting in series expect in the case Vu> 2Vdc/3. In both +Ve and –Ve cycle the 4 power electronic switches are conducting. So we can say that the switching losses will be reduced due to less number of conducting switches.

The drawback of the proposed seven level inverter is that the voltage rating of the full bridge converter is higher than that of conventional multilevel inverter topology. The leakage current is an important parameter in a solar power generation system for transformerless operation. The leakage current is dependent on the parasitic capacitance and the negative terminal voltage of the solar cell array respect to ground . To reduce the leakage current, the filter inductor Lf should be replaced by a symmetric topology and the solar power generation system is redrawn as shown in the below Fig FIG:

**PROPOSED SOLAR POWER GENERATION SYSTEM FOR SUPRESSING THE LEAKAGE CURRENTS**
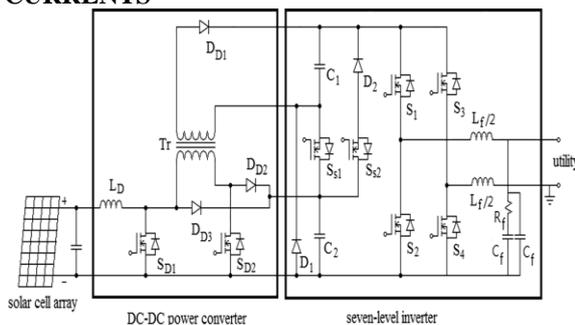


**CONTROLLING FOR BOOST CONVERTER AND POWER INVERTER**
In this proposed system we are having dc-dc power converter and a 7- level inverter. The dc-dc power converter feeds the inverter with capacitance providing two independent voltage sources with multiple relationships and performs maximu8m power point tracking (MPPT) in order to extract the maximum output power from the solar cell array. The 7-level inverter converts the capacitance voltage into a high range A.C Voltage for utility voltage system.

In order to perform the operation of the boost converter and inverter perfectly we are constructing a controlling system for both the converter and inverter.
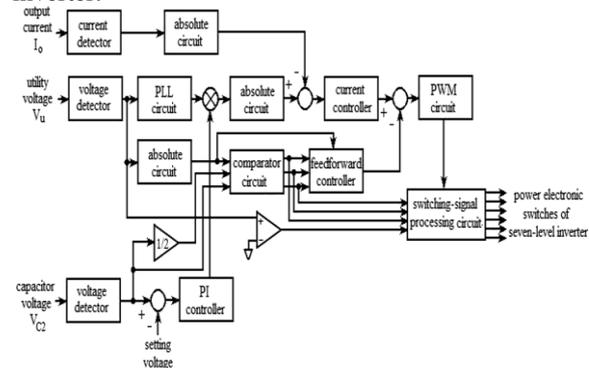


(a)
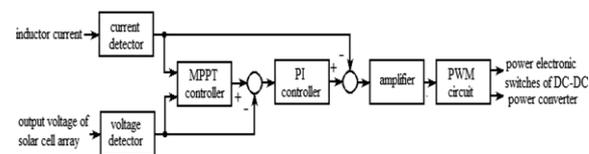


(b)

**FIG(8): CONTROL SCHEME FOR (a) 7-LEVEL INVERTER (b) DC-DC POWER CONVERTER**

**A.7-LEVEL INVERTER**
Fig. 8(a) shows the control block diagram for the seven-level inverter. The control object of the seven-level inverter is its output current, which should be sinusoidal and in phase with the utility voltage. The utility voltage is detected by a voltage detector, and then sent to a phase-lock loop (PLL) circuit in order to generate a sinusoidal signal with unity amplitude. The voltage of capacitor C2 is detected and then compared with a setting voltage. The compared result is sent to a PI controller.
Then, the outputs of the PLL circuit and the PI controller are sent to a multiplier to produce the reference signal, while the output current of the seven-level inverter is detected by a current detector. The reference signal and the detected output current are sent to absolute circuits and then sent to a subtractor, and the output of the subtractor is sent to a current controller. The detected utility

voltage is also sent to an absolute circuit and then sent to a comparator circuit, where the absolute utility voltage is compared with both half and whole of the detected voltage of capacitor C2 , in order to determine the range of the operating voltage. The comparator circuit has three output signals, which correspond to the operation voltage ranges, (0, Vdc/3), (Vdc/3, 2Vdc/3), and (2Vdc/3, Vdc). The feed-forward control eliminates the disturbances of the utility voltage, Vdc/3 and 2Vdc/3,. The absolute value of the utility voltage and the outputs of the compared circuit are sent to a feed- forward controller to generate the feed- forward signal. Then, the output of the current controller and the feed-forward signal are summed and sent to a PWM circuit to produce the PWM signal. The detected utility voltage is also compared with zero, in order to obtain a square signal that is synchronized with the utility voltage. Finally, the PWM signal, the square signal, and the outputs of the compared circuit are sent to the switching signal processing circuit to generate the control signals for the power electronic switches of the seven- level inverter, according to Table I. The current controller controls the output current of the seven level inverter, which is a sinusoidal signal of 60 Hz. Since the feed- forward control is used in the control circuit, the current controller can be a simple amplifier, which gives good tracking performance. As can be seen in (6), (8), and (10), the gain of the current controller determines the bandwidth and the steady state error. The gain of the current controller must be as large as possible in order to ensure a fast response and a low steady-state error. But the gain of the current controller is limited because the bandwidth of the power converter is limited by the switching frequency.

**B. DC–DC Power Converter**
Fig. 8(b) shows the control block diagram for the dc–dc power converter. The input for the DC-DC power converter is the output of the solar cell array. A ripple voltage with a frequency that is double that of the utility appears in the voltages of C1 and C2 , when the seven-level inverter feeds real power into the utility. The MPPT function is degraded if the output voltage of solar cell array contains a ripple voltage. Therefore, the ripple voltages in C1 and C2 must be blocked by the dc–dc power converter to provide improved MPPT. Accordingly, dual control loops, an outer voltage control loop and an inner current control loop, are used to control the dc–dc power converter. Since the output voltages of the DC-DC power converter comprises the voltages of C1 and C2 , which are controlled by the seven-level inverter, the outer voltage control loop is used to regulate the output voltage of the solar cell array.

The inner current control loop controls the inductor current so that it approaches a constant current and blocks the ripple voltages in C1 and C2 . The perturbation and observation method is used to provide MPPT [24]. The output voltage of the solar cell array and the inductor current are detected and sent to a MPPT controller to determine the desired output voltage for the solar cell array. Then the detected output voltage and the desired output voltage of the solar cell array are sent to a subtractor and the difference is sent to a PI controller. The output of the PI controller is the reference signal of the inner current control loop. The reference signal and the detected inductor current are sent to a subtractor and the difference is sent to an amplifier to complete the inner current control loop. The output of the amplifier is sent to the PWM circuit. The PWM circuit generates a set of complementary signals that control the power electronic switches of the dc–dc power converter.

**EXPERIMENTAL ANALYSIS**
The power rating of the prototype is 500 W, and the prototype was used for a single- phase utility with 110Vand 50 Hz. Table II shows the main parameters of the prototype. Figs. 9 and 10 show the experimental results for the seven level inverter when the output power of solar power generation system is 500 W. Fig. 9 shows the experimental results for the AC side of the seven-level inverter. Fig. 9(b) shows that the output voltage of the seven-level inverter has seven voltage levels. The output current of the seven-level inverter, shown in Fig. 9(c), is sinusoidal and in phase with the utility voltage, which means that the grid-connected power conversion interface feeds a pure real power to the utility. The total harmonic distortion (THD) of the output current of the seven-level inverter is 3.6%. Fig. 10 shows the experimental results for the dc side of the seven-level inverter. Fig. 10(b) and (c) show that the voltages of capacitors C2 and C1 of the capacitor selection circuit have multiple relationships and are maintained at 60 and 120 V, respectively. Fig. 10(d) shows that the output voltage of the capacitor selection circuit has three voltage levels (60, 120, and 180 V). Fig. 11shows the experimental results for the dc–dc power converter. Fig. 11(b) and (c) shows that the ripple voltages in capacitors C1 and C2 of the capacitor selection circuit are evident. However, the ripple current in the inductor of the dc–dc power converter is less than 0.5 A when the average current of inductor is 8 A, as shown in Fig. 11(a). Therefore, the ripple voltages in C1 and C2 are blocked by the dc–dc power converter. Fig. 12 shows the output power scan for the solar cell array when the output voltage

changes from 40 to 70 V. Fig. 13 shows the experimental results for the beginning of MPPT for the dc–dc converter. Fig. 13 shows that the output power of the solar cell array is almost constant when maximum power tracking is achieved and its value is very close to the maximum power shown in Fig. 12. Fig. 14 shows the experimental results for the power efficiency of the proposed solar power generation system. The solar cell array was replaced by a dc power supply to simplify the adjustment of output power in the experimental process. With higher step-up gain of the dc–dc power converter, there is lower power efficiency. Hence, the higher input voltage of solar power generation system will result in better power efficiency of the dc–dc power converter. Since a transformer is used in the dc–dc power converter of the proposed solar power generation system, this degrades the power efficiency of the proposed solar power generation system. However, the power transferred by the transformer is less than one third of the solar output power in the proposed dc–dc power converter, and the energy stored in the magnetizing inductance of the transformer is transferred forward to the output capacitor. Hence, the degradation of power efficiency caused by use of the transformer in the proposed solar power generation system is not serious
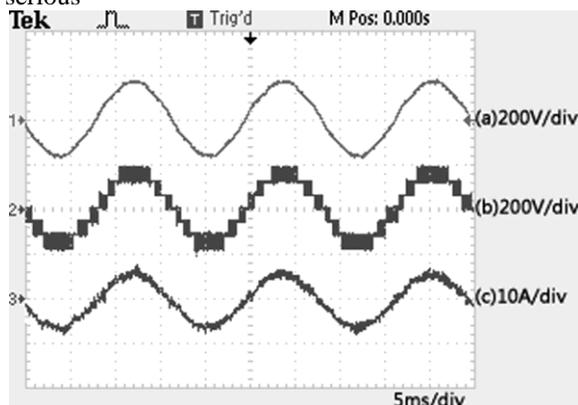


**FIG(9): Experimental results for tha ac side of the seven- level inverter.(a) Utility Voltage,(b) output voltage of seven-level inverter, and (c) output current of the seven- level inverter**
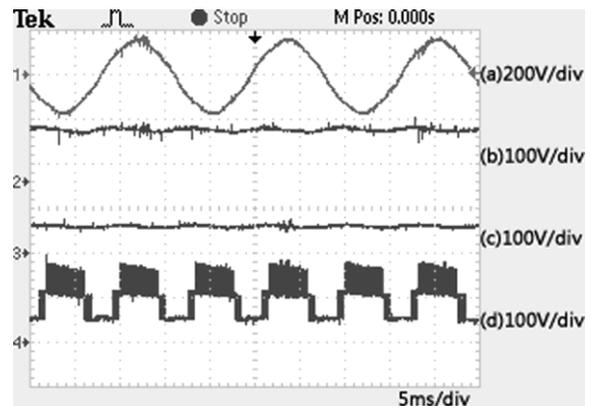


**FIG(10): Experimental results for the dc side of the seven- level inverter (a) utility Voltage, (b) voltage of capacitor c2, (c) voltage of capacitor c1, and (d) output voltage of the capacitor selection circuit.**
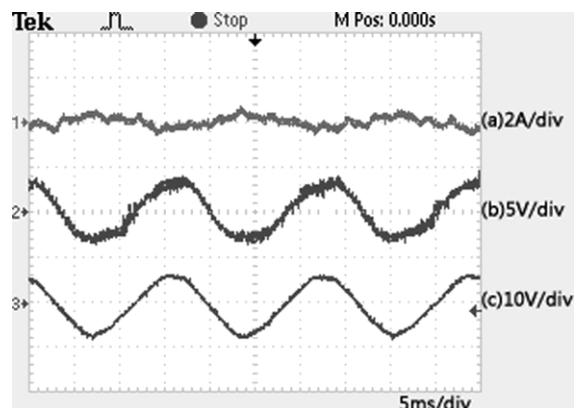


**FIG(11): Experimental result of the DC-DC power converter (a) ripple current of inductor. (b) ripple voltage of capacitor c2, and (c) ripple voltage of capacitor c1**

## VI.    CONCLUSION

This paper proposes a solar power generation system to convert the dc energy generated by a solar cell array into ac energy that is fed into the utility. The proposed solar power generation system is composed of a dc–dc power converter and a seven level inverter. The seven-level inverter contains only six power electronic switches, which simplifies the circuit configuration. Furthermore, only one power electronic switch is switched at high frequency at any time to generate the seven-level output voltage. This reduces the switching power loss and improves the power efficiency. The voltages of the two dc capacitors in the proposed seven-level inverter are balanced automatically, so the control circuit is simplified. Experimental results show that the proposed solar power generation system generates a seven-level output voltage and outputs a sinusoidal current that is in phase with the utility voltage, yielding a power factor of unity. In addition, the

proposed solar power generation system can effectively trace the maximum power of solar cell array.

## REFERENCES

[1] J.-M. Shen, H. L. Jou, and J. C. Wu, "Novel transformer-less gridconnected power converter with negative grounding for photovoltaic generation system," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1818–1829, Apr. 2012

[2] M. Chaves, E. Margato, J. F. Silva, and S. F. Pinto, "New approach in back-to-back m-level diodeclamped multilevel converter modelling and direct current bus voltages balancing," IET power Electron., vol. 3, no. 4,pp. 578–589, 2010.

[3] K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multicell converter based on modified phase-shifted pulsewidth modulation," IEEE Trans. Power Electron., vol. 25, no. 6,pp. 1517–1526, Jun. 2010.

[4] X. She, A. Q. Huang, T. Zhao, and G. Wang, "Coupling effect reduction of a voltage- balancing controller in single-phase cascaded multilevel converters,"IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3530–3543, Aug. 2012.

[5] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics Converters, Applications and Design, Media Enhanced 3rd ed. New York, NY, USA: Wiley, 2003.

[6] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energybalance control of PV cascaded multilevel grid-connected inverters under level-shifted and phase-shifted PWMs," IEEE Trans. Ind. Electron., vol. 60, no. 1, pp. 98–111, Jan. 2013.

[7] J. M. Shen, H. L. Jou, and J. C. Wu, "Novel transformer-less gridconnected power converter with negative grounding for photovoltaic generation system," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1818–1829, Apr. 2012.

[8] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," IEEE Trans. Power Electron., vol. 20, no. 4, pp. 963–973, Jul. 2005.

[9] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," IEEE Trans. Ind. Electr., vol. 58, no. 6, pp. 2435–2443, Jun. 2011.

[10] Y. Ounejjar, K. Al-Hadded, and L. A. Dessaint, "A novel six-band hysteresis control for the packed U cells seven-level converter: Experimental validation," IEEE Trans. Ind. Electron., vol. 59, no. 10, pp. 3808–3816,Oct. 2012.

[11] I.Abdalla, J. Corda, and L. Zhang, "Multilevel DC-link inverter and control algorithm to overcome the PV partial shading," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 11–18, Jan. 2013.

**C.PRAVEEN** received B.Tech degree in EEE from SKIT engineering college, Srikalahasti in 2009, M.Tech degree in Electrical power systems from SVPCET college, Puttur in 2012 and currently working as an Asst.Professor in Department of EEE, CREC, Tirupati, Andhra Pradesh, India.

**P. Kishore raju** born in Andhra Pradesh, India in 1991. He received his bachelor degree in electrical and electronics engineering(EEE) in 2012 from GKCE engineering college. He is currently pursuing his master of technology on power electronics and drives (Pe&D) in CREC Tirupati Andhra Pradesh. His research interest includes on power electronic devices and their application in power systems.